



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Eliyahou Harari et al.
Title: Non-Volatile Memory Cells Utilizing Substrate Trenches
Application No.: 09/925,134 Filing Date: August 8, 2001
Examiner: Quinto, Kevin V. Group Art Unit: 2826
Docket No.: SNDK.111US1 Conf. No.: 6957

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) call(s) the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 are enclosed.

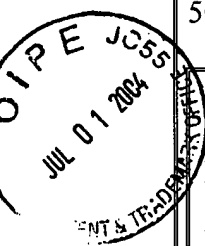
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EV437668638US

Respectfully submitted,

Gerald P. Parsons
Reg. No.: 24,486

July 1, 2004

Date

PARSONS HSUE & DE RUNTZ LLP
655 Montgomery Street, Suite 1800
San Francisco, CA 94111
(415) 318-1160 (main)
(415) 318-1163 (direct)
(415) 693-0194 (fax)

Attorney Docket No.: SNDK.111US1
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U.S. Department of Commerce, Patent and Trademark Office		Atty Docket No.	Serial No.
		M-10237-1P US	09/92134
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)	
(Use several sheets if necessary)		Eliyahou Harari; Jack H.Yuan; George Samachisa, Henry Chien.	
		Filing Date	Group
		August 8, 2001	2814

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	1	5,891,774	4/6/1999	Ueda et al.			
	2	5,786,612	7/28/1998	Otani et al.			
	3	5,606,521	2/25/1997	Kuo et al.			
	4	5,616,510	4/1/1997	Wong			
	5	5,643,814	7/1/1997	Chung			
	6	5,486,714	1/23/1996	Hong			
	7	5,495,441	2/27/1996	Hong			
	8	5,498,564	3/12/1996	Geissler et al.			
	9	5,576,567	11/19/1996	Mori			
	10	5,411,905	5/2/1995	Acovic et al.			
	11	5,315,142	5/24/1994	Acovic et al.			
	12	6,391,716	5/21/02	Liou			
	13	5,168,334	12/1/92	Mitchell et al.			

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	14	10041414	2/13/1998	Japan			Abstr.	
	15	252221	7/21/1995	Taiwan			Abstr.	
	16	03-042873	2/25/1991	Japan			Abstr.	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

17	Ogura et al. "Low Voltage, Low Current, High Speed Program step split gate Cell with Ballistic Direct Injection for EEPROM/Flash," <u>IEEE Publication</u> , 9/1998, pp. 36.5.1-36.5.4.
18	Di-Son Kuo et al. , "TEFET--A High Density, Low Erase Voltage, Trench Flash EEPROM," <u>IEEE Publication</u> , 4/1994, pp. 51-52.
19	Pein et al. , "Performance of the 3-D Sidewall Flash EPROM Cell," <u>Syposium on VLSI Technology Digest of Technical Papers (IEEE)</u> , 11/1993, pp. 2.1.1-2.1.4.

Examiner

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.